SRINIVASA RAMANUJAN INSTITUTE OF TECHNOLOGY
(Autonomous)
Affiliated to JNTUA & Approved by AICTE
Accredited by NAAC with 'A' Grade & Accredited by NBA (CSE, ECE & EEE)
Rotarypuram Village, B K Samudram Mandal, Ananthapuramu – 515701.

OUTCOME BASED EDUCATION
WITH
CHOICE BASED CREDIT SYSTEM

MASTER OF TECHNOLOGY

VLSI DESIGN

COURSE STRUCTURE AND SYLLABI SRIT R23

M. Tech. Regular Two Year PG Degree Program
(Effective for the students admitted from the academic year 2019 – 2020)

These rules and regulations may be altered/changed from time to time by the Academic Council

FAILURE TO READ AND UNDERSTAND THE RULES IS NOT AN EXCUSE

Course Structure
(Based on AICTE Model Curriculum)
SRIT-R23

Master of Technology
in
VLSI Design

M. Tech. Course Structure

I Semester

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DVLSI101	CMOS Analog IC Design	PC	3	0	0	3	40	60	100
23DVLSI102	CMOS Digital IC Design	PC	3	0	0	3	40	60	100
23DVLSI103a 23DVLSI103b 23DVLSI103c	Program Elective – I Microchip Fabrication Techniques Nanomaterials and Nanotechnology CAD for VLSI	PE	3	0	0	3	40	60	100
23DVLSI104a 23DVLSI104b 23DVLSI104c	Program Elective – II Device Modelling FPGA Architectures and Applications ASIC Design	PE	3	0	0	3	40	60	100
23DVLSI105	CMOS Analog IC Design Lab	PC	0	0	4	2	40	60	100
23DVLSI106	CMOS Digital IC Design Lab	PC	0	0	4	2	40	60	100
23DRM101	Research Methodology and IPR	MC	2	0	0	2	40	60	100
23DAC101a 23DAC101b 2D3AC101c	Audit Course – I English for Research paper writing Disaster Management Sanskrit for Technical Knowledge	AC	2	0	0	0	40	-	40
					Total	18	320	420	740

L-Lecture, T-Tutorial, P-Practical

II Semester

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DVLSI201	CMOS Mixed Signal IC Design	PC	3	0	0	3	40	60	100
23DVLSI202	Physical Design Automation	PC	3	0	0	3	40	60	100
23DVLSI203a 23DVLSI203b 23DVLSI203c	Program Elective – III SoC Testing and Verification Semiconductor Memory Design and Testing MEMS System Design	PE	3	0	0	3	40	60	100
23DVLSI204a 23DVLSI204b 23DVLSI204c	Program Elective – IV Low Power VLSI Design IoT and its Applications VLSI Signal Processing	PE	3	0	0	3	40	60	100
23DVLSI205	CMOS Mixed Signal IC Design Lab	PC	0	0	4	2	40	60	100
23DVLSI206	Physical Design Automation Lab	PC	0	0	4	2	40	60	100
23DVLSI207	Technical Seminar	PR	0	0	4	2	100	-	100
23DAC201a 23DAC201b 23DAC201c	Audit Course – II Pedagogy Studies Stress Management for Yoga Personality Development through Life Enlightenment Skills	AC	2	0	0	0	40	-	40
					Total	18	380	360	740

L-Lecture, T-Tutorial, P-Practical

III Semester

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DVLSI301a 23DVLSI301b 23DVLSI203c	Program Elective – V Bi-CMOS Technology and Applications Optimization Techniques and Applications in VLSI Design SoC Architecture	PE	3	0	0	3	40	60	100
23DOE301b 23DOE301c 23DOE301e	Open Elective – I Industrial Safety Business Analytics Waste to Energy	OE	3	0	0	3	40	60	100
23DVLSI302	Dissertation Phase – I	PR	0	0	20	10	100	-	100
23DVLSI303	Co-curricular Activities	-	0	0	0	2	40	-	40
					Total	18	220	120	340

L-Lecture, T-Tutorial, P-Practical

IV Semester

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DVLSI401	Dissertation Phase – II	PR	0	0	32	16	-	100	100
					Total	16	-	100	100

L-Lecture, T-Tutorial, P-Practical

Program Elective-I

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DVLSI103a	Microchip Fabrication Techniques	PE	3	0	0	3	40	60	100
23DVLSI103b	Nanomaterials and Nanotechnology	PE	3	0	0	3	40	60	100
23DVLSI103c	CAD for VLSI	PE	3	0	0	3	40	60	100

Program Elective-II

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DVLSI104a	Device Modelling	PE	3	0	0	3	40	60	100
23DVLSI104b	FPGA Architectures and Applications	PE	3	0	0	3	40	60	100
23DVLSI104c	ASIC Design	PE	3	0	0	3	40	60	100

Program Elective-III

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DVLSI203a	SoC Testing and Verification	PE	3	0	0	3	40	60	100
23DVLSI203b	Semiconductor Memory Design and Testing	PE	3	0	0	3	40	60	100
23DVLSI203c	MEMS System Design	PE	3	0	0	3	40	60	100

Program Elective-IV

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DVLSI204a	Low Power VLSI Design	PE	3	0	0	3	40	60	100
23DVLSI204b	IoT and its Applications	PE	3	0	0	3	40	60	100
23DVLSI204c	VLSI Signal Processing	PE	3	0	0	3	40	60	100

Program Elective-V

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DVLSI301a	Bi-CMOS Technology and Applications	PE	3	0	0	3	40	60	100
23DVLSI301b	Optimization Techniques and Applications in VLSI Design	PE	3	0	0	3	40	60	100
23DVLSI203c	SoC Architecture	PE	3	0	0	3	40	60	100

Open Elective-I

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DOE301b	Industrial Safety	OE	3	0	0	3	40	60	100
23DOE301c	Business Analytics	OE	3	0	0	3	40	60	100
23DOE301e	Waste to Energy	OE	3	0	0	3	40	60	100

Audit Course-I

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DAC101a	English for Research Paper Writing	AC	2	0	0	0	40	-	40
23DAC101b	Disaster Management	AC	2	0	0	0	40	-	40
2D3AC101c	Sanskrit for Technical Knowledge	AC	2	0	0	0	40	-	40

Audit Course-II

Course Code	Course Name	Subject Area	Periods per week			Credits	Scheme of Examination (Max. Marks)		
			L	T	P		CIA	SEE	Total
23DAC201a	Pedagogy Studies	AC	2	0	0	0	40	-	40
23DAC201b	Yoga for Stress Management	AC	2	0	0	0	40	-	40
23DAC201c	Personality Development through Life Enlightenment Skills	AC	2	0	0	0	40	-	40

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**CMOS ANALOG IC DESIGN**	**L**	**T**	**P**	**C**
23DVLSI101		**3**	**0**	**0**	**3**

Course Objectives:

- This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
- Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- Intuitive understanding and real-life applications are emphasized throughout the course.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two- Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.
- To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

UNIT - I

Basic MOS Device Physics: General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

UNIT - II

Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Current Steering Circuit

UNIT - III

Frequency Response of Amplifiers: General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT - IV

Feedback Amplifiers: General Considerations, Feedback Topologies, Effect of Loading. OperationalAmplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection,Noise in Op Amps, Stability and Frequency Compensation.

UNIT - V

Comparators: Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Textbooks:

1. B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition2016.
2. Paul.R.Gray& Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.

Reference Books:

1. T.C.Carusone, D.A.Johns&K.Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012.
2. P.E.Allen & D.R.Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
3. R.Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.
4. Adel S. Sedra, Kenneth C. Smith, Arun, "Microelectronic Circuits", 6th Edition, Oxford University Press.

Course Outcomes:

CO1: Understand the different testing and design methodologies of semiconductor memory.
CO2: Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories.
CO3: Build fault models for memory testing.
CO4: Analyze different parameters that lead malfunctioning of memories.
CO5: Design reliable memories with efficient architecture to improve processes times and power.
CO6: Analysis of memory technologies and operations of different semiconductor memories.

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**CMOS DIGITAL IC DESIGN**	**L**	**T**	**P**	**C**
23DVLSI102		**3**	**0**	**0**	**3**

Course Objectives:

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

UNIT - I

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT - II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT - III

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT - IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT - V

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Textbooks:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Edition, PHI.

Course Outcomes:

CO1: Understand the fundamental areas of applications for the integrated Çircuits
CO2: Study and analyze the performance of CMOS Inverter circuits on the basis of their operation and working.
CO3: Relate, compare, interpret and make the use of the best CMOS design techniques for implementation, analysis & design of Combinational MOS logic circuits.
CO4: Relate, compare, interpret and make the use of the best CMOS design techniques for implementation, analysis & design of Sequential MOS logic circuits.
CO5: Define, simplify & justify which dynamic logic circuit can be used investigate CMOS circuits.
CO6: Know & tell different types of memories and compare performance evaluation of each memory modules so they can be able to think & justify how to improve performance by taking different structures.

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**MICROCHIP FABRICATION TECHNIQUES**	**L**	**T**	**P**	**C**
23DVLSI203a	**Program Elective – I**	**3**	**0**	**0**	**3**

Course Objectives:

- Comprehend impact of semiconductor industry on the design of development of integratedcircuits.
- Acquaint with clean room technology
- Understand oxidation methods, aspects of photolithography, diffusion, ion implantationtechniques.
- Specify NMOS and CMOS design rules corresponding to 180nm, 90nm and45nm technologies
- Understand packaging principles

UNIT - I

Introduction to Processing: Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction.

UNIT - II

Photolithography: Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hardbake, develop inspect, Dry etching Wet etching, resist stripping.

UNIT - III

Diffusion & Ion Implantation: Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT - IV

Film Depositions and Growth: Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT - V

Yield: Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors.
Packaging: Chip characteristics, package functions, package operations.

Textbooks:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall, 2000.

Reference Books

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

Course Outcomes:

CO1:Explain the basic concepts of microchip fabrication techniques
CO2:Explain the stages of fabrication processing
CO3:Explain the stages involved in photo lithography
CO4:Illustrate the process of diffusion and implantation
CO5:Illustrate the process of film depositions
CO6:Explain packaging techniques and design rules

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**NANOMATERIALS AND NANOTECHNOLOGY**	**L**	**T**	**P**	**C**
23DVLSI203b	**Program Elective – I**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand the basic idea behind the design and fabrication of nano scale systems.
- To understand and formulate new engineering solutions for current problems and technologiesfor future applications.
- To acquire knowledge on the operation of fabrication and characterization devices to achieveprecisely designed systems.

UNIT - I

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive– hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

UNIT - II

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials. Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low DimensionalCarbon-Related Nanomaterials.

UNIT - III

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

UNIT - IV

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT"s - Multi-walled nanotubes, Single-walled nano tubes Optical properties of CNT"s, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNTs.

UNIT - V

Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane-based application, polymer-based application.

Textbooks:

1. Kenneth J.Klabunde and Ryan M.Richards, "Nanoscale Materials in Chemistry", 2ndedition,John Wiley and Sons, 2009.
2. I Gusev and A Rempel, "Nanocrystalline Materials", Cambridge International Science Publishing, 1stIndian edition by Viva Books Pvt. Ltd. 2008.
3. B.S.Murty,P.Shankar,Baldev Raj, B.B.Rath, James Murday, "Nanoscience and Nanotechnology",Tata McGrawHill Education 2012.

Reference Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. Digital Integrated Circuits - A Design Perspective, Jan M.Rabaey, An ant Chandrakasan, Borvivoje Nikolic, 2nd Edition, PHI.

Course Outcomes:

CO1: Understand the concept of nano materials and nanotechnologies, features of nano structures, Classification of nanomaterials, Micro electro mechanical Systems (MEMS), Synthesis of CNTs, mechanisms of CNTs and Ferroelectric materials
CO2: Explain the features of nanostructures, Applications of nano materials and technologies and Nano dimensional Materials 0D, 1D, 2D structures.
CO3: Understand the Classification of Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials and its applications.
CO4: Illustrate the Micro electro mechanical Systems (MEMS) and Nanolithography Techniques,

Emerging Applications, Nano Phonics.

CO5: Demonstrate the Synthesis of CNTs, mechanisms of CNT"s, Electrical transport in perfect nanotubes.

CO6: Explain the Ferroelectric materials and Nano electronics, biological, environmental, membranes.

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**CAD FOR VLSI**	**L**	**T**	**P**	**C**
23DVLSI203c	**Program Elective – I**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification.
- To demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement.
- To practice the application of fundamentals of VLSI technologies
- To optimize the implemented design for area, timing and power by applying suitable constraints.

UNIT - I

Introduction: VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT - II

Partitioning: Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.

UNIT - III

Floor Planning: Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT - IV

Placement and Routing: Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT - V

Physical Design Automation of FPGAs and MCMs: FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

Textbooks:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

Course Outcomes:

CO1: Explain the various phases of CAD for digital electronic systems, from VLSI design cycle to partitioning, floor planning, and physical design Physical Design Automation of FPGAs and MCMs.
CO2: Explain the VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle and System Packaging Styles.
CO3: Illustrate the concept of Partitioning, Pin Assignment and Placement along with Simulated Annealing.
CO4: Demonstrate the Floor Planning, Classification of floor planning algorithms and also constraint-based floor planning.
CO5: Explain the Placement, Classification of placement algorithms, Partitioning based placement algorithms and Routing, Global Routing and Detailed Routing for application of fundamentals of VLSI technologies.
CO6: Illustrate the Physical Design Automation of FPGAs, Physical Design cycle for FPGAs and MCM Physical Design Cycles.

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**DEVICE MODELLING**	**L**	**T**	**P**	**C**
23DVLSI104a	**Program Elective – II**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand the physics of 2-terminal MOS operation and its characteristics
- To understand the physics of 4-terminal MOSFET operation and its characteristics.
- To analyze the SOI MOSFET electrical characteristics.

UNIT - I

2-terminal MOS device: threshold voltage modelling (ideal case as well as considering the effects of Qf, Φms and Dit.).

UNIT - II

C-V characteristics (ideal case as well as taking into account the effects of Qf, Φms and Dit);MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit)

UNIT - III

4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT - IV

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model)

UNIT - V

SOI MOSFET: Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics.

Textbooks:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nanotransistors, World Scientific Publishing Co Pte Ltd 2017.

Reference Books

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Trasistors, Academic Press, 1995.
3. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009

Course Outcomes:

CO1:Describe the behavior of all components successfully.
CO2: Understand the physics of 2-terminal MOS operation and its characteristics.
CO3: Analyze the operation and modeling of the MOS Capacitor.
CO4:Understand the physics of 4-terminal MOSFET operation and its characteristics.
CO5:Understand the design elements of MOSFETs.
CO6:Analyze the SOI MOSFET electrical characteristics.

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**FPGA ARCHITECTURES AND APPLICATIONS**	**L**	**T**	**P**	**C**
23DVLSI104b	**Program Elective – II**	**3**	**0**	**0**	**3**

Course Objectives:

- To acquire knowledge about various architectures and device technologies of PLD's.
- To comprehend FPGA Architectures.
- To analyze System level Design and their application for Combinational and SequentialCircuits.
- To familiarize with Anti-Fuse Programmed FPGAs.
- To apply knowledge of this subject for various design applications.

UNIT - I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Coo Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT - II **Field Programmable Gate Arrays**

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT - III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT - IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT - V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

Textbooks:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer InternationalEdition.
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

Reference Books:

1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier,Newnes.
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

Course Outcomes:

CO1: Understand the programmable logic devices, organisation of FPGAs and the role of FPGAs in real-time signal processing applications.
CO2: Acquire knowledge about various architectures and device technologies of PLD's.
CO3: Comprehend FPGA Architectures.
CO4: Analyze System level Design and their application for Combinational and Sequential Circuits.
CO5: Familiarize with Anti-Fuse Programmed FPGAs.
CO6: Apply knowledge of this subject for various design applications.

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**ASIC DESIGN**	**L**	**T**	**P**	**C**
23DVLSI104c	**Program Elective – II**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand different types of ASICs and their libraries.
- To understand about programmable ASICs, I/O modules and their interconnects.
- To familiarize different methods of software ASIC design their simulation, testing andconstruction of ASICs.

UNIT - I

Introduction to ASICs: Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT - II

Programmable ASICs and Programmable ASIC Logic Cells: The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT - III

I/O Cells and Interconnects & Programmable ASIC Design Software: DC Output, AC Output,DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT - IV

Low Level Design Entry and Logic Synthesis: Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the viterbi decoder.

UNIT - V

Simulation, Test and ASIC Construction: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, the importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in
Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods

Textbooks:

1. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson Education,2003.
2. L.J.Herbst, "Integrated Circuit Engineering", Oxford Science Publications, 1996.

Reference Books:

1. HimanshuBhatnagar, "Advanced ASIC Chip Synthesis using Synopsis Design Compiler", 2nd Edition, Kluwer Academic, 2001.

Course Outcomes:

CO1: understand different types of ASIC like Xilinx,ALTERA etc.,
CO2: Understand the various types of Application-Specific Integrated Circuits (ASICs), including Gate-Array, Standard Cell, and Data Path Cell designs
CO3: Understand the fundamental concepts and principles behind Programmable ASICs, including Antifuse, Static RAM, EPROM, and EEPROM technologies.
CO4: Understand I/O Cells and Interconnects, Xilinx I/O Block and Other I/O Cells& Integration of programmable ASIC design software tools into the design.
CO5: Understand Low-Level Design Entry, Low-Level Design Languages& Application of PLA Tools.
CO6: Understand various types of simulations used in digital design& the principles of FPGA partitioning.

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**CMOS ANALOG IC DESIGN LAB**	**L**	**T**	**P**	**C**
23DVLSI105		**0**	**0**	**4**	**2**

Course Objectives:

- To explain the VLSI Design Methodologies using VLSI design tool.
- To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
- To explain the Physical Verification in Layout Design
- To fully appreciate the design and analyze of analog and mixed signal simulation
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

List of Experiments:

- The students are required to design and implement any **TEN** Experiments using CMOS 130nmTechnology.
- The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:

Software:

Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

Course Outcomes (CO):

CO1: Explain the VLSI Design Methodologies using VLSI design tool.
CO2: Grasp the significance of various CMOS analog circuits in full-custom IC Design flow
CO3: Understand the Physical Verification in Layout Design practically.
CO4: Fully appreciate the design and analyze of analog and mixed signal simulation
CO5: Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation for amplifiers, op-amp circuits and A/D and D/A converters.
CO6: Enhance their understanding of CMOS devices and analog circuit design principles,preparing them for practical applications in the field of integrated circuit design.

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**CMOS DIGITAL IC DESIGN LAB**	**L**	**T**	**P**	**C**
23DVLSI106		**0**	**0**	**4**	**2**

Course Objectives:

- To explain the VLSI Design Methodologies using any VLSI design tool.
- To grasp the significance of various design logic Circuits in full-custom IC Design.
- To explain the Physical Verification in Layout Extraction.
- To fully appreciate the design and analyze of CMOS Digital Circuits.
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

The students are required to design and implement the Circuit and Layout of any **TEN** Experiments using CMOS 130nm Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software:

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

Course Outcomes:

CO1:Make use of hardware description language for the design, verification and simulation of CMOS logic gates circuits. **(Apply)**

CO2:Make use of hardware description language for the design and simulation of CMOS combinational logic circuits. **(Apply)**

CO3:Make use of hardware description language for the design and simulation of CMOS sequential logic circuits, Static RAM Cell, Dynamic Logic Circuits. **(Apply)**

CO4:Explain the CMOS Digital Design Methodologies using any VLSI design tool. (Understand)

CO5:Develop the Design and simulation of various digital logic Circuits in full-custom IC Design that involves recognizing their pivotal role in shaping the circuit's functionality. **(Apply)**

CO6:Explain the Physical Verification in Layout Extraction and fully appreciate the design and analyze of CMOS Digital Circuits. **(Understand)**

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**RESEARCH METHODOLOGY AND IPR**	**L**	**T**	**P**	**C**
23DRM101		**2**	**0**	**0**	**2**

Course Objectives:

- Identify an appropriate research problem in their interesting domain.
- Understand ethical issues understand the Preparation of a research project thesis report.
- Understand the Preparation of a research project thesis report
- Understand the law of patent and copyrights.
- Understand the Adequate knowledge on IPR

UNIT - I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

UNIT - II

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, howto write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT - III

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT - IV

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases.Geographical Indications.

UNIT - V

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Textbooks:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science &engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

Reference Books:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide forbeginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in NewTechnological Age", 2016.

Course Outcomes:

CO1: Develop a comprehensive understanding of research methodology, intellectual property rights and their applications in diverse fields.
CO2: select appropriate approaches for investigating and solving research problems, including data collection, analysis, and interpretation techniques.
CO3: develop a well-structured research proposal, including its format, and present and defend it in front of a review committee.
CO4: Analyse the international scenario of intellectual property, understanding the importance of global collaboration in this field.
CO5: Analyse licensing and technology transfer processes, understanding their role in the commercialization of intellectual property.
CO6: Analyse case studies related to traditional knowledge and IPR, understanding its implications on educational and research institutions, specifically IITs.

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**CMOS MIXED SIGNAL IC DESIGN**	**L**	**T**	**P**	**C**
23DVLSI201		**3**	**0**	**0**	**3**

Course Objectives:

- To demonstrate first order filter with least interference
- To extend the concept of phase locked loop for designing PLL application with minimumjitter by considering non ideal effects.
- To design different A/D, D/A, modulators, demodulators and different filter for real timeapplications

UNIT - I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks,Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators, first order filters, Switch sharing, biquad filters.

UNIT – II

Phased Lock Loop (PLL) : Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT - III

Data Converter: Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters,Hybrid converters

UNIT - IV

A to D Converters: Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Sigma Delta A/D converters, Time- interleaved converters.

UNIT - V

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters,Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A

Textbooks:

1. Design of Analog CMOS Integrated Circuits- BehzadRazavi, TMH Edition, 2002.
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013.

Reference Books:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003.
2.Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inter science, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience,2009.

Course Outcomes:

CO1: Explain the basic concepts of CMOS Mixed signal IC Design
CO2: Illustrate the operation and characteristic analysis of switched capacitor circuits
CO3: Explain the working of phase locked loop and its types
CO4: Illustrate the types of converters with their specifications
CO5: Explain the working of A to D converter models
CO6: Classify the types of oversampling converters

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**PHYSICAL DESIGN AUTOMATION**	**L**	**T**	**P**	**C**
23DVLSI202		**3**	**0**	**0**	**3**

Course Objectives:

- To understand relation between automation algorithms and constraints posed by VLSItechnology.
- To adopt algorithms to meet critical design parameters.
- To design area efficient logics by employing different routing algorithms and shape functions.
- To simulate and synthesis different combinational and sequential logics.

UNIT - I

VLSI Design Automation Tools: Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

UNIT - II

Layout: Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

UNIT - III

Floor planning and routing: Floor planning concepts, Shape functions and floor planning sizing,Local routing, Area routing, Channel routing, global routing and its algorithms.

UNIT - IV

Simulation and Logic Synthesis: Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, constructionand manipulation, two level logic synthesis.

UNIT - V

High-Level Synthesis: Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment,High level transformations.

Textbooks:

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998.
2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999.

Reference Books:

1. S.M. Sait,H.Youssef, VLSI Physical Design Automation, World scientific, 1999.
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

Course Outcomes:

CO1:Describe the automation process for VLSI system design .
CO2: Understand of VLSI Design Automation.
CO3: Acquire knowledge about CAD tools used for VLSI design.
CO4: Able to understanding Algorithms for VLSI Design Automation.
CO5: Able to gather knowledge of High-Level Synthesis.
CO6: Understand Timing Analysis

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**SoC TESTING AND VERIFICATION**	**L**	**T**	**P**	**C**
23DVLSI203a	**Program Elective – III**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand the concepts of faults and testing in SoC
- To implement the faults using simulation tools
- To analyze BIST systems

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSITesting, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation.

UNIT - III

Testability Measures: SCOAP Controllability and Observablity, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self-Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Textbooks:

1. M.L. Bushnell, V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Pulishers.
2. M. Abramovici, M.A.Breuer and A.D Friedman, "Digital Systems and Testable Design", Jaico Publishing House.

Reference Books:

1. P.K. Lala, "Digital Circuits Testing and Testability", Academic Press.

Course Outcomes:

CO1: Prepare to tackle testing and verification challenges in modern SoC design, facilitating the creation of dependable and high-performance integrated circuits.
CO2: Develop the foundational knowledge and analytical skills essential for effective testing in the domain of VLSI..
CO3: Develop the simulation techniques for verifying SoC designs and evaluating test effectiveness.
CO4: Develop the testability measures, with a focus on SCOAP, controllability, and observability in the context of SoC design.
CO5: Understand the design and operation of test-per-clock and test-per-scan BIST systems in the context of SoC testing.
C06: Learn how to use boundary scan test instructions and navigate pin constraints specific to SoC design.

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**SEMICONDUCTOR MEMORY DESIGN AND TESTING**	**L**	**T**	**P**	**C**
23DVLSI203b	**Program Elective – III**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand different types of memories, their architectural and different packingtechniques of memories.
- To build fault models for memory testing.
- To analyze different parameters that lead malfunctioning of memories.
- To design reliable memories with efficient architecture to improve processes times and power.

UNIT - I

Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT - II

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOSPROMS, EPROM, Floating gate EPROM cell, One-time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM orEEPROM), advanced Flash memory architecture

UNIT - III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory.

UNIT - IV

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures.

UNIT - V

Advanced Memory Technologies and High-density Memory Packing Technologies
Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

Textbooks:
1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley. 2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma, 2002, Wiley.
Reference Books:
1. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, First Edition. Prentice all.
Course Outcomes:
CO1: Understand the different testing and design methodologies of semiconductor memory. CO2: Get complete knowledge regarding different types of memories, their architectural and different packing techniques of memories. CO3: Build fault models for memory testing. CO4: Analyze different parameters that lead malfunctioning of memories. CO5: Design reliable memories with efficient architecture to improve processes times and power. CO6: Analysis of memory technologies and operations of different semiconductor memories.

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**MEMS SYSTEM DESIGN**	**L**	**T**	**P**	**C**
23DVLSI203c	**Program Elective – III**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand the basic concepts of MEMS technology and working of MEMS devices.
- To understand and select different materials for current MEMS devices and competingtechnologies for future applications.
- To understand the concepts of fabrication process of MEMS, Design and Packaging Methodology.
- To analyze the various fabrication techniques in the manufacturing of MEMS Devices.

UNIT - I

Introduction to MEMS: Introduction to MEMS & Real world Sensor/Actuator examples (DMD, Air-bag, pressure sensors).MEMS Sensors in Internet of Things (IoT), Bio-Medical Applications

UNIT - II

MEMS Materials and Their Properties: Materials (eg. Si, SiO2, SiN, Cr, Au, Ti, SU8, PMMA, Pt); Important properties: Young modulus, Poisson's ratio, density, piezo-resistive coefficients, TCR,Thermal Conductivity, Material Structure. Understanding Selection of materials based on applications.

UNIT - III

MEMS Fab Processes – 1: Understanding MEMS Processes & Process parameters for: Cleaning, Growth & Deposition, Ion Implantation & Diffusion, Annealing, Lithography. Understanding selection of Fab processes based on Applications.

UNIT - IV

MEMS Fab Processes – 2: Understanding MEMS Processes & Process parameters for: Wet & Dry etching, Bulk& Surface Micromachining, Die, Wire& Wafer Bonding, Dicing, Packaging. Understanding selection of Fab processes based on Applications.

UNIT - V

MEMS Devices: Architecture, working and basic quantitative behaviour of Cantilevers, Micro heaters, Accelerometers, Pressure Sensors, Micro mirrors in DMD, Inkjet printer-head. Understanding steps involved in Fabricating above devices.

Textbooks:

1. An Introduction to Micro electromechanical Systems Engineering; 2nd Edition by N.Maluf, K Williams; Publisher: Artech House Inc
2. Practical MEMS - by Ville Kaajakari; Publisher: Small Gear Publishing
3. Micro system Design - by S. Senturia; Publisher: Springer

Reference Books:

1. Analysis and Design Principles of MEMS Devices –Minhang Bao; Publisher: Elsevier Science.
2. Fundamentals of Micro fabrication - by M. Madou; Publisher:CRC Press; 2ndedition
3. Micro Electro Mechanical System Design - by J. Allen; Publisher: CRC Press 4.
4. Micro machined Transducers Sourcebook - by G. Kovacs; Publisher: McGraw-Hill.

Course Outcomes:

CO1: Explain the basic concepts of MEMS, MEMS Material Properties, MEMS Fab Processes and MEMS Devices.
CO2: Illustrate the MEMS Sensors in Internet of Things (IoT) and Bio-Medical Applications
C03: Classify the different materials and their properties for current MEMS devices and competing technologies for future applications.
CO4: Demonstrate the concepts of fabrication process of MEMS, design and Packaging Methodology.
CO5: Explain the various fabrication techniques in the manufacturing of MEMS Devices.
CO6: Illustrate the Architecture, working and basic quantitative behavior of Cantilevers and Micro mirrors in DMD.

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**LOW POWER VLSI DESIGN**	**L**	**T**	**P**	**C**
23DVLSI204a	**Program Elective – IV**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- To implement Low power design approaches for system level and circuit level measures.
- To design low power adders, multipliers and memories for efficient design of systems.

UNIT - I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT - II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach–Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT - III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT - IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT - V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Textbooks:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

Course Outcomes:

CO1: understand the low-power VLSI circuit design fundamental principles, techniques, low power design approaches, Low-Voltage Low-Power Adders, Low-Voltage Low-Power Multipliers and Low-Voltage Low-Power Memories.
CO2: significance of low-power circuit design and its applications, static and dynamic power dissipation sources and short channel effects.
CO3: Implement the low power circuits through Voltage Scaling Techniques, Architectural Level Approaches and to minimize the switched capacitance.
CO4: Design the Low-Voltage Low-Power Adders through standard adder cell and technological trends for power supply voltage.
CO5: Analyse the Low-Voltage Low-Power Multipliers through different multiplier architectures and

Wallace Tree Multiplier. CO6: analyse the design procedure for ROM,SRAM and DRAM circuits.

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**IOT AND ITS APPLICATIONS**	**L**	**T**	**P**	**C**
23DVLSI204b	**Program Elective – IV**	**3**	**0**	**0**	**3**

Course Objectives:

- To apply the Knowledge in IOT Technologies and Data management.
- To determine the values chains Perspective of M2M to IOT.
- To implement the state of the Architecture of an IOT.
- To compare IOT Applications in Industrial & real world.
- To demonstrate knowledge and understand the security and ethical issues of an IOT.

UNIT - I

Fundamentals of IoT: Evolution of Internet of Things, Enabling Technologies, IoT Architectures, one M2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.
IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT - II

IoT Protocols: IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT - III

Design and Development: Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT - IV

Data Analytics and Supporting Services: Structured Vs Unstructured Data and Data in Motion VsData in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka,
Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT - V

Case Studies/Industrial Applications: IoT applications in home, infrastructures, buildings, security,Industries, Home appliances, other IoT electronic equipment's. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded targetboards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino).

Textbooks:

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.

2. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madisetti, Universities Press,2015

Reference Books:

1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).
2. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence", Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.
3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.

Course Outcomes:

CO1: Discuss the Fundamentals concepts used in IoT Technologies. (Understand)
CO2: Explain the Architecture of an IoT with IoT interdependence Technologies and IoT hardware Platforms. (Understand)
CO3: Interpret the networking concepts and protocols involved in IoT development. (Understand)
CO4: Make use of the Arduino and RaspberryPi on-chip peripherals for configuring and programming to implement IoT applications. (Apply)
CO5: Explain the Data Analytics and Supporting cloud Services in Data management for IoT :Applications and its security. (Understand)
CO6: Compare the IoT Applications in Industrial and real world. (Understand)

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**VLSI SIGNAL PROCESSING**	**L**	**T**	**P**	**C**
23DVLSI204c	**Program Elective – IV**	**3**	**0**	**0**	**3**

Course Objectives:

- To study the existing architectures suitable for VLSI.
- To understand the concepts of folding and unfolding algorithms and applications.
- To design new architectures suitable for VLSI.
- To implement fast convolution algorithms.

UNIT - I

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT - II

Folding and Unfolding: Folding- Introduction, Folding Transform, register minimization Techniques, register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfoldingand Retiming, Applications of Unfolding.

UNIT - III

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT - IV

Fast Convolution: Introduction – Cook - Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT - V

Low Power Design: Digital lattice filter structures, bit level arithmetic, architecture, redundantarithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, Scaling
Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

Textbooks:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science, 1998.
2. Kung S. Y, H. J. While House, T. Kailath ,VLSI and Modern Signal processing , Prentice Hall, 1985.

Reference Books

1. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing , Prentice Hall, 1994.
2. Medisetti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), 1995

Course Outcomes:

CO1:acquired the knowledge and skills needed to effectively design, analyze, and optimize digital signal processing systems with a focus on low-power considerations.
CO2: Demonstrate the ability to represent DSP algorithms, ensuring clarity and precision in their description.
CO3: Develop folding transform, register minimization techniques, algorithms for unfolding and retiming methods for solving system inequalities.
CO4: Analyse the principles of systolic array design for FIR filters and space representations containing delays.
CO5: Develop fast convolution algorithms through inspection, showcasing their ability to optimize convolution processes.
CO6: analyse the architecture and applications of digital lattice filter structures, demonstrating their understanding of bit-level arithmetic and redundant arithmetic.

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**CMOS MIXED SIGNAL IC DESIGN LAB**	**L**	**T**	**P**	**C**
23DVLSI205		**0**	**0**	**4**	**2**

Course Objectives:

- To design and simulate op-amp for given specifications
- To design and simulate data converter for given specifications
- To design and simulate PLL and VCO for given specifications
- To understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.

List of Experiments:

The students are required to design and implement the Circuit and Layout of the following Experiments using CMOS 130nm Technology.

Cycle 1:

1) Fully compensated op-amp with resistor and miller compensation
2) High speed comparator design
   a. Two stage cross coupled clamped comparator
   b. Strobed Flip-flop
3) Data converter

Cycle 2:

1) Switched capacitor circuits
   a. Parasitic sensitive integrator
   b. Parasitic insensitive integrator
2) Design of PLL
3) Design of VCO
4) Band gap reference circuit
5) Layouts of All the circuits Designed and Simulated

Software:

Mentor Graphics/ Cadence/ Tanner/Industry Equivalent Standard Software Tools

Hardware:

Personal Computer with necessary peripherals, configuration and operating System.

References:

1. David A johns, Ken Martin, Analog Integrated Circuit Design, Wiley, 2008.
2. R. Gregorian and G.C Ternes, Analog MOS Integrated Circuits for Signal Processing,Wiley,1986.
3. Roubik Gregorian, Introduction to CMOS Op-Amp and Comparators, Wiley, 1999.
4. Alan Hastlings, The art of Analog Layout, Wiley, 2005.

Course Outcomes (CO):

CO1: Acquire hands-on experience in designing and implementing advanced circuits using CMOS 130nm technology.
CO2: Design and simulate op-amp for given specifications
CO3: Design and simulate data converter for given specifications
CO4: Design and simulate PLL and VCO for given specifications
CO5: Understand the Significance of Pre-Layout Simulation and Post-Layout Simulation.
CO6: Draw layout designs for all circuits developed and simulated during the experiments

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**PHYSICAL DESIGN AUTOMATION LAB**	**L**	**T**	**P**	**C**
23DVLSI206		**0**	**0**	**4**	**2**

Course Objectives:

- To learn the implementation of different Physical Design Automation algorithms
- To implement different graph algorithms
- To implement different partitioning algorithms
- To implement different floor planning algorithms
- To implement different routing algorithms

List of Experiments:

Cycle 1:

1) Graph algorithms
   a) Graph search algorithms
      i. Depth first search
      ii. Breadth first search
   b) Spanning tree algorithm
      i. Kruskal"s algorithm
   c) Shortest path algorithm
      i. Dijkstra algorithm
      ii. Floyd- Warshall algorithm
   d) Steiner tree algorithm
2) Computational geometry algorithm
   a) Line sweep method
   b) Extended line sweep method

Cycle 2:

3) Partitioning algorithms
   a) Group migration algorithms
      I. Kernighan –Lin algorithm
      II. Extensions of Kernighan-Lin algorithm
         i) Fiduccias –Mattheyses algorithm
         ii) Goldberg and Burstein algorithm
   b) Simulated annealing and evolution algorithms
      i. Simulated annealing algorithm
      ii. Simulated evolution algorithm
   III) Metric allocation method

4) Floor planning algorithms
   i) Constraint based methods
   ii) Integer programming based methods
   iii) Rectangular dualization based methods
   iv) Hierarchical tree based methods

v) Simulated evolution algorithms
vi) Time driven Floor planning algorithms

5) Routing algorithms
I) Two terminal algorithms
a) Maze routing algorithms
i) Lee"s algorithm
ii) Soukup"s algorithm
iii) Hadlock algorithm
b) Line-Probe algorithm
c) Shortest path-based algorithm
II) Multi terminal algorithm
a) Stenier tree-based algorithm
i) SMST algorithm
ii) Z-RST algorithm

Software required: C/C++ Programming Language /Relevant software

Text Books:

1) Naveed Shervani, Algorithms for Physical Design Automation, 3rd Edition, Kluwer Academic,1998.
2) Charles J Alpert, Dinesh P Mehta, Sachin S. Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press,2008.

Course Outcomes (CO):

CO1: Learn the implementation of different Physical Design Automation algorithms
CO2: Implement different graph algorithms
CO3: Implement different partitioning algorithms
CO4: Implement different floor planning and routing algorithms
CO5: Understanding and practical experience in a variety of algorithms used in graph theory, computational geometry, partitioning, and floor planning.
CO6: Acquire skills in algorithm design, implementation, and analysis.

M.Tech(VLSI Design)- III Semester					SRIT-R23
Course Code	**BICMOS TECHNOLOGY AND APPLICATIONS**	**L**	**T**	**P**	**C**
23DVLSI301a	**Program Elective – V**	**3**	**0**	**0**	**3**

Course Objectives:

- To demonstrate in-depth knowledge in BiCMOS Technology.
- To analyze complex engineering problems critically for conducting research in BiCMOS Technology.
- To solve engineering problems with wide range of solutions in Radio Frequency Integrated circuits.
- To realize different digital circuits using BiCMOS Technology

UNIT - I

BiCMOS Process Technology: CMOS Process Technology, Bipolar Process Technology, Isolation in CMOS and Bipolar Technologies, BiCMOS Technology, BiCMOS Design Rules.

UNIT - II

Device Design Considerations: Design Considerations for MOSFET's, Design Considerations for Bipolar Transistors, BiCMOS Device Design Considerations.
BiCMOS Device Scaling: MOS Device Scaling, Bipolar Device Scaling.

UNIT - III

Device Modeling: Modeling of the MOS Transistor: MOSFET Structure and Operation, SPICE Models of the MOS Transistor, Analytical Model for Short-Channel MOS Devices.
Modeling of the Bipolar Transistor: BJT Structure and Operation, Ebers-Moll Model, Bipolar Models in SPICE.

UNIT - IV

BiCMOS Digital Integrated Circuits: BiMOS Totem-Pole Inveter: DC Characteristics, Transient Analysis, Delay Dependence on the Device Parameters, BiCMOS Circuit Design, Comparing CMOS and BiCMOS Inverters Speed, BiCMOS Gates.

UNIT - V

BiCMOS Digital Circuit Applications: Adders, Multiplier, Random Access Memory, Programmable Logic Arrays, BiCMOS Logic Cells, BiCMOS Gate Arrays.

Textbooks:

1. Sherif H.K. Embabi, AbdellatifBellaouar& Mohamed I. Elmasry "Digital BiCMOS Integrated Circuit Design" Springer Science+ BusÎness Media, LLC.
2. A L ALVAREZ, BICMOS Technology & Applications, Kluwer Academic Publishers.

Reference Books:

1.Kiat-Seng yeo, Samir S. Rofail, Wang-Ling Goh, CMOS/BiCMOS ULSI, Pearson Education.
2.James C. Daly, Denis P. Galipeau, Analog BiCMOS Design: Practices & Pitfalls, CRC Press
3.KlaasJan de Langen, Johan Huijsing, Compact Low-Voltage and High-Speed CMOS, BiCMOS and Bipolar Operational Amplifiers, Springer Science

Course Outcome:

CO1-Explain the basic concepts of Bi-CMOS technology
CO2-Illustrate the BiCMOS processing and design rules
CO3-Explain the device design considerations and scaling parameters of MOSFET and BJT
CO4-Explain the device modelling of MOS transistor
CO5-Illustrate the characteristics of BiCMOS Digital Integrated Circuit
CO6-Explain the industrial applications BiCMOS Digital Circuit

M.Tech(VLSI Design)- III Semester					SRIT-R23
Course Code	**OPTIMIZATION TECHNIQUES AND APPLICATIONS**	**L**	**T**	**P**	**C**
23DVLSI301b	**IN VLSI DESIGN (Program Elective – V)**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand basics of statistical modeling
- To analyze performance of CMOS circuits with respect to power, area and speed
- To acquire complete knowledge regarding the various algorithms used for optimization of power and area

UNIT - I

Statistical Modeling: Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom's model, Principal component- based modeling, Quad tree- based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT - II

Statistical Performance, Power and Yield Analysis: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and powersupply variations, High level yield estimation and gate level yield estimation.

UNIT - III

Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting-Monomial fitting, Max monomial fitting, Polynomial fitting.

UNIT - IV

Genetic Algorithm: Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, mapping for FPGA-Automatic test generation-Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS- Standard cell placement GASP algorithm-unified algorithm.

UNIT - V

GA Routing Procedures and Power Estimation: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation- application of GA Standard cell placement – GA for ATG-problem encoding-fitness function-GA Vs Conventional algorithm.

Textbooks:

1. Statistical Analysis and Optimization for VLSI: Timing and Power –Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation -Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.

Reference Books:

1.Convex Optimization- Stephen Boyd, Lieven Vandenberghe, Cambridge University Press,2004

Course Outcome:

CO1: Explain the Convex Optimization, Statistical Performance, Power and Yield Analysis, Statistical Modeling, Genetic Algorithm, GA Routing Procedures and Power Estimation.
C02: Explain the Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom's model and Principal component modeling.
CO3: Illustrate the concept of Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models and power supply variations, High level yield estimation and gate level yield estimation.
CO4: Demonstrate the Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, generalized geometric programming and fitting-Monomial fitting, Max monomial fitting, Polynomial fitting.
CO5: Explain the GA Technology-Steady State Algorithm-Fitness Scaling Inversion GA for VLSI

Design, Layout and Test automation- partitioning-automatic placement, routing technology, mapping for FPGA-Automatic test generation-Partitioning algorithm. C06: Illustrate the Global routing-FPGA technology mapping circuit generation-test generation in a GA frame work-test generation procedures and Power estimation.

M.Tech(VLSI Design)- III Semester					SRIT-R23
Course Code	**SoC ARCHITECTURE**	**L**	**T**	**P**	**C**
23DVLSI203c	**Program Elective – V**	**3**	**0**	**0**	**3**

Course Objectives:

- To understand the basics related to SoC architecture and different approaches related to SoC Design
- To select an appropriate robust processor for SoC Design.
- To select an appropriate memory for SoC Design.
- To realize real time case studies.

UNIT - I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory & Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT - II

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT - III

Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV

Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT - V

Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation;Image compression–JPEG compression.

Textbooks:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.

Reference Books:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer.
2. Co-Verification of Hardware and Softwarefor ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Patersonand Leena Singh L, 2001, Kluwer Academic Publishers.

Course Outcome:

CO1: Explain the basic SoC architecture design
CO2: Explain the hardware and software system approach for SoC Design
CO3: Explain the elements involved in processor selection for SoC design
CO4: Illustrate the types of Memory used for SoC deign
CO5: Explain the interconnect and configuration for the SoC deign
CO6: Illustrate the case studies involving the applications of SoC design

AUDIT COURSE-I

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**ENGLISH FOR RESEARCH PAPER WRITING**	**L**	**T**	**P**	**C**
23DAC101a		**2**	**0**	**0**	**0**

Course Objectives: This course will enable students:

- Understand the essentials of writing skills and their level of readability.
- Learn about what to write in each section.
- Ensure qualitative presentation with linguistic accuracy.

Course Outcomes (CO): Student will be able to

- Understand the significance of writing skills and the level of readability.
- Analyze and write title, abstract, different sections in research paper.
- Develop the skills needed while writing a research paper.

UNIT - I

1Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breaking up Long Sentences-Structuring Paragraphs and Sentences-Being Concise and Removing Redundancy -Avoiding Ambiguity

UNIT - II

Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Cauterization

UNIT - III

Introducing Review of the Literature – Methodology - Analysis of the Data-Findings - Discussion-Conclusions-Recommendations.

UNIT - IV

Key skills needed for writing a Title, Abstract, and Introduction

UNIT - V

Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and drawConclusions

Suggested Reading

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books) Model Curriculum of Engineering & Technology PG Courses [Volume-I]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**DISASTER MANAGEMENT**	**L**	**T**	**P**	**C**
23DAC101b		**2**	**0**	**0**	**0**

Course Objectives: This course will enable students:

- Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice fromMultiple perspectives.
- Developanunderstandingofstandardsofhumanitarianresponseandpracticalrelevanceinspecific typesof disasters and conflict situations
- Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

UNIT - I

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics

UNIT - II

Repercussions of Disasters and Hazards:

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches,Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT - III

Disaster Preparedness and Management:

Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT - IV

Risk Assessment Disaster Risk:

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation.Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT - V

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Suggested Reading

1. R.Nishith,Singh AK, "Disaster Management in India: Perspectives ,issues and strategies.
2. "'New Royal book,
   Company. Sahni, Pardeep Et.Al.(Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Ha ll Of India, New Delhi.
3. Goel S.L., Disaster Administration And Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi

M.Tech(VLSI Design)- I Semester					SRIT-R23
Course Code	**SANSKRITFOR TECHNICAL KNOWLEDGE**	**L**	**T**	**P**	**C**
23DAC101c		**2**	**0**	**0**	**0**

Course Objectives: This course will enable students:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing thememory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge
- Knowledge from ancient literature

Course Outcomes (CO): Student will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science &technology can be understood
- Being a logical language will help to develop logic in students

UNIT - I	
Alphabets in Sanskrit,	
UNIT - II	
Past/Present/Future Tense, Simple Sentences	
UNIT - III	
Order, Introduction of roots	
UNIT - IV	
Technical information about Sanskrit Literature	
UNIT - V	
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics	

Suggested Reading

1. "Abhyaspustakam" –Dr.Vishwas, Sanskrit-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha- Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd.,New Delhi

AUDIT COURSE-II

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**PEDAGOGY STUDIES**	**L**	**T**	**P**	**C**
23DAC201a		**2**	**0**	**0**	**0**

Course Objectives: This course will enable students:

- Reviewexistingevidenceonthereviewtopictoinformprogrammedesignandpolicy makingundertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes (CO): Student will be able to

Students will be able to understand:

- Whatpedagogicalpracticesarebeingusedbyteachersinformalandinformalclassrooms in developingcountries?
- What is the evidence on the effectiveness of these pedagogical practices, in whatconditions, and with what population of learners?
- Howcanteachereducation(curriculumandpracticum)andtheschoolcurriculumand guidancematerials best support effective pedagogy?

UNIT - I

Introduction and Methodology: Aims and rationale, Policy back ground, Conceptual frame work and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and searching.

UNIT - II

Thematic overview: Pedagogical practices are being used by teachers in formal and informalclassrooms in developing countries. Curriculum, Teacher education.

UNIT - III

Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessmentof included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT - IV

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head Teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large classsizes

UNIT - V

Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

Suggested Reading

1. AckersJ,HardmanF(2001)ClassroominteractioninKenyanprimaryschools,Compare, 31 (2): 245-261.
2. AgrawalM(2004)Curricularreforminschools:Theimportanceofevaluation,Journalof
3. Curriculum Studies, 36 (3): 361-379.
4. AkyeampongK(2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
5. Akyeampong K, LussierK, PryorJ, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
6. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education.Oxford and Boston: Blackwell.
   Chavan M (2003) Read India: A mass scale, rapid, 'learning to read 'campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**STRESSMANAGEMENT BY YOGA**	**L**	**T**	**P**	**C**
23DAC201b		**2**	**0**	**0**	**0**

Course Objectives: This course will enable students:

- To achieve overall health of body and mind
- To overcome stres

Course Outcomes (CO): Student will be able to

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT - I

Definitions of Eight parts of yog.(Ashtanga)

UNIT - II

Yam and Niyam.

UNIT - III

Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramha charya and aparigrahaii)
Shaucha,santosh,tapa, swadhyay, ishwarpranidhan

UNIT - IV

Asan and Pranayam

UNIT - V

i) Various yoga poses and their benefits for mind &body
ii) Regularization of breathing techniques and its effects-Types of pranayam

Suggested Reading

1. 'Yogic Asanas for GroupTarining-Part-I": Janardan SwamiYogabhyasiMandal, Nagpur
2. "Rajayogaor conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata

M.Tech(VLSI Design)- II Semester					SRIT-R23
Course Code	**PERSONALITY DEVELOPMENT THROUGHLIFE ENLIGHTENMENTSKILLS**	**L**	**T**	**P**	**C**
23DAC201c		**2**	**0**	**0**	**0**
	Semester	**II**			

Course Objectives: This course will enable students:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes (CO): Student will be able to

- StudyofShrimad-Bhagwad-Geetawillhelpthestudentindevelopinghispersonalityand achievethe highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT - I

Neetisatakam- Holistic development of personalityVerses-19,20,21,22(wisdom)
Verses-29,31,32(pride &heroism)
Verses-26,28,63,65(virtue)

UNIT - II

Neetisatakam- Holistic development of personality Verses-52,53,59(dont's)
Verses-71,73,75,78(do's)

UNIT - III

Approach to day-to-day work and duties.
Shrimad Bhagwad Geeta: Chapter2-Verses41,47,48,
Chapter3-Verses13,21,27,35, Chapter 6-
Verses5,13,17,23,35, Chapter18-Verses45,46,48.

UNIT - IV

Statements of basic knowledge.
Shrimad Bhagwad Geeta: Chapter2-Verses
56,62,68 Chapter12 -Verses13,14,15,16,17,18
Personality of Role model. Shrimad Bhagwad Geeta:

UNIT - V

Chapter2-Verses 17,Chapter3-
Verses36,37,42,Chapter4-Verses18,38,39
Chapter18– Verses37,38,63

Suggested Reading

1. "Srimad Bhagavad Gita "by Swami Swarupa nanda Advaita Ashram (Publication Department), Kolkata
2. Bhartri hari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

OPEN ELECTIVE

M.Tech(VLSI Design)- III Semester					SRIT-R23
Course Code	**INDUSTRIAL SAFETY**	**L**	**T**	**P**	**C**
23DOE301b		**3**	**0**	**0**	**3**

Course Objectives:

- To know about Industrial safety programs and toxicology, Industrial laws , regulations and sourcemodels
- To understand about fire and explosion, preventive methods, relief and its sizing methods
- To analyse industrial hazards and its risk assessment.

Course Outcomes (CO): Student will be able to

- To list out important legislations related to health, Safety and Environment.
- To list out requirements mentioned in factories act for the prevention of accidents.
- To understand the health and welfare provisions given in factories act.

UNIT - I

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types,causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety,wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety colorcodes. Fire prevention and firefighting, equipment and methods.

UNIT - II

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy,Service life of equipment.

UNIT - III

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants- types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT - IV

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault-finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii.Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT - V

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance.
Repair cycle concept and importance

Textbooks:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

Reference Books:

1. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

M.Tech(VLSI Design)- III Semester					SRIT-R23
Course Code	**BUSINESS ANALYTICS**	**L**	**T**	**P**	**C**
23DOE301c		**3**	**0**	**0**	**3**

Course Objectives:

- The main objective of this course is to give the student a comprehensive understanding of business analytics methods.

Course Outcomes (CO): Student will be able to

- Students will demonstrate knowledge of data analytics.
- Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
- Students will demonstrate the ability to use technical skills in predicative andprescriptive modeling to support business decision-making.
- Students will demonstrate the ability to translate data into clear, actionable insights.

UNIT - I

Business Analysis: Overview of Business Analysis, Overview of Requirements, Role of the Business Analyst.
Stakeholders: the project team, management, and the front line, Handling Stakeholder Conflicts.

UNIT - II

Life Cycles: Systems Development Life Cycles, Project Life Cycles, Product Life Cycles, Requirement Life Cycles.

UNIT - III

- Forming Requirements: Overview of Requirements, Attributes of Good Requirements, Types of Requirements, Requirement Sources, Gathering Requirements from Stakeholders, Common Requirements Documents. Transforming Requirements: Stakeholder Needs Analysis, Decomposition Analysis,Additive/Subtractive Analysis, Gap Analysis, Notations (UML & BPMN), Flowcharts, Swim Lane Flowcharts, Entity-Relationship Diagrams, State-Transition Diagrams, Data Flow Diagrams, Use Case.
- Modeling, Business Process Modeling

UNIT - IV Lecture Hrs:

Finalizing Requirements: Presenting Requirements, Socializing Requirements and Gaining Acceptance, Prioritizing Requirements. Managing Requirements Assets: Change Control, Requirements Tools

UNIT - V

Recent Trands in: Embedded and colleborative business intelligence, Visual data recovery, Data Storytelling and Data Journalism.

Textbooks:

1. Business Analysis by James Cadle et al.
2. Project Management: The Managerial Process by Erik Larson and, Clifford Gray

Reference Books:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G.Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

M.Tech(VLSI Design)- III Semester					SRIT-R23
Course Code	**WASTE TO ENERGY**	**L**	**T**	**P**	**C**
23DOE301e		**3**	**0**	**0**	**3**

Course Objectives:

- Introduce and explain energy from waste, classification and devices to convert waste toenergy.
- To impart knowledge on biomass pyrolysis, gasification, combustion and conversion process.
- To educate on biogas properties ,bio energy system, biomass resources and their classificationand biomass energy programme in India.

Course Outcomes (CO): Student will be able to

- To know about overview of Energy to waste and classification of waste.
- To acquire knowledge on bio mass pyrolysis, gasification, combustion and conversion processin detail.
- To gain knowledge on properties of biogas, biomass resources and programmes to convertwaste to energy in India.

UNIT - I

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue,Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT - II

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT - III

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT - IV

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT - V

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification -Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification- pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production -Urban waste to energy conversion - Biomass energy programme in India.

Textbooks:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 2018
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., TMH, 2017

Reference Books:

1. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
2. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley& Sons, 1996.
3. **Online Learning Resources:**
https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ch13/
https://www.youtube.com/watch?v=x2KmjbCvKTk